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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,029	02/25/2004	Daniel Boyko	A0312.70513US00	3915

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,029	BOYKO ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10-18 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 10 recites the limitation "the core circuitry" in line 14 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 25 recites the limitation "the first value" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims 11-18 are also rejected due to the limitations of the base claims and any intervening claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 3, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Sullam et al. (U.S. Patent No. 6,614,320).

In reference to claim 1, Sullam discloses in Figure 2 a device having a clock generation circuit (112) which produces a first clock signal (output of 214) for use in timing internal circuitry and a second clock timing circuitry that interfaces to external circuitry, the clock generation circuit comprising: a) a phase locked loop (213, 212) having an output, b) a first programmable frequency scaling circuit (214) having an input coupled to the output of the phase locked loop (213, 212), an output of the first programmable frequency scaling circuit (214) providing the first clock signal; and c) a second programmable frequency scaling circuit (218) having an input coupled to the output of the phase locked loop (213, 212), an output of the second programmable frequency scaling circuit (218) supplying the second clock signal. The same applies to claim 10.

In reference to claim 2, Sullam discloses in Figure 1 that the device additionally comprises a) digital logic (102) receiving as a clock input the first clock; and b) interface logic (114), interfacing to the digital logic components external to the device and receiving as a clock input the second clock signal (see also Figure 2).

In reference to claim 3, Sullam discloses in Figure 2 that the first and second programmable frequency scaling circuits are programmable dividers.

7. Claims 1, 2, 3, 8, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimoda et al. (U.S. Patent No. 6,675,249).

In reference to claim 1, Shimoda discloses in Figure 3 a device having a clock generation circuit which produces a first clock signal (CLK) for use in timing internal circuitry and a second clock timing circuitry that interfaces to external circuitry, the clock generation circuit comprising: a) a phase locked loop (240) having an output, b) a first programmable frequency scaling circuit (244) having an input coupled to the output of the phase locked loop (240), an output of the first programmable frequency scaling circuit (244) providing the first clock signal; and c) a second programmable frequency scaling circuit (254) having an input coupled to the output of the phase locked loop (240), an output of the second programmable frequency scaling circuit (254) supplying the second clock signal (BUSCLK). The same applies to claim 10.

In reference to claim 2, Shimoda discloses in column 1, lines 60-65 that the device additionally comprises a) digital logic (L2 cache) receiving as a clock input the first clock (CLK, the internal clock); and b) interface logic (external bus interface), interfacing to the digital logic components external to the device and receiving as a clock input the second clock signal (BUSCLK).

In reference to claim 3, Shimoda discloses in Figure 3 that the first and second programmable frequency scaling circuits are programmable dividers.

In reference to claim 8, Shimoda discloses in Figure 3 that the phase locked loop (240) additionally comprises a third programmable divider (241).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-7, 9, 12-13, 16-20, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sullam et al. (U.S. Patent No. 6,614,320) in view of Petersson et al. (U.S. Patent No. 5,140,284).

In reference to claim 5, Sullam discloses all the limitations of the base claims (1, 10) and any intervening claims as mentioned above. Sullam does not disclose the control logic. Petersson discloses in Figure 2 control logic (27) providing control signals to multiple programmable dividers (21, 25, 26). It would have been obvious to one skilled in the art that the method of controlling the programmable dividers of Petersson could have been used in the circuit of Sullam for controlling the programmable dividers of that circuit for the advantage of being able to achieve quick lock-in combined with low noise/interference levels and additionally being able to switch reference frequencies without generating phase jumps (as disclosed by Petersson in column 2, lines 21-26). The same applies to claim 9, 18, and 22 (see Sullam column 1, lines 49-55) and claim 19 (see Petersson column 3, lines 15-44).

In reference to claim 4, it is considered well known to one skilled in the art that dividers may be implemented using counters, of which fact official notice is taken. The same applies to claim 23.

In reference to claim 6, Petersson discloses in column 3, lines 41-44 that the control logic (27) is able to provide to the first programmable divider a control signal controlling the loading of a programmed divider value, when the control logic detects an end of a period of the first clock (see column 3, lines 15-44). The same applies to claim 7.

In reference to claim 12, Petersson discloses in Figure 2 the ability to change the first frequency ratio (this is done by control circuit 27) such that the first circuitry is clocked at a lower rate (which is seen to be the power saving mode called for in the claim). The same applies to claim 13, wherein the frequency of the reference clock (f_{ref}) can also be reduced to form a second power saving mode. The same also applies to claims 16-17 and 20 wherein the values of the frequency dividers may be changed separately and the values chosen can be chosen so that the frequencies of the first and second clock are not integer multiples of each other. The same also applies to claim 24, wherein the limitation of using the circuit in a battery operated electronic device is seen to be intended use and is therefore not given any patentable weight.

10. Claims 4-7, 9, 12-13, 16-20, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda et al. (U.S. Patent No. 6,675,249) in view of Petersson et al. (U.S. Patent No. 5,140,284).

In reference to claim 5, Shimoda discloses all the limitations of the base claims (1, 10) and any intervening claims as mentioned above. Shimoda does not disclose the control logic. Petersson discloses in Figure 2 control logic (27) providing control signals to multiple programmable dividers (21, 25, 26). It would have been obvious to one

skilled in the art that the method of controlling the programmable dividers of Petersson could have been used in the circuit of Shimoda for controlling the programmable dividers of that circuit for the advantage of being able to achieve quick lock-in combined with low noise/interference levels and additionally being able to switch reference frequencies without generating phase jumps (as disclosed by Petersson in column 2, lines 21-26). The same applies to claim 9, 18, and 22 (wherein the circuit is seen to comprise a semiconductor chip) and claim 19 (see Petersson column 3, lines 15-44).

In reference to claim 4, it is considered well known to one skilled in the art that dividers may be implemented using counters, of which fact official notice is taken. The same applies to claim 23.

In reference to claim 6, Petersson discloses in column 3, lines 41-44 that the control logic (27) is able to provide to the first programmable divider a control signal controlling the loading of a programmed divider value, when the control logic detects an end of a period of the first clock (see column 3, lines 15-44). The same applies to claim 7.

In reference to claim 12, Petersson discloses in Figure 2 the ability to change the first frequency ratio (this is done by control circuit 27) such that the first circuitry is clocked at a lower rate (which is seen to be the power saving mode called for in the claim). The same applies to claim 13, wherein the frequency of the reference clock (f_{ref}) can also be reduced to form a second power saving mode. The same also applies to claims 16-17 and 20 wherein the values of the frequency dividers may be changed separately and the values chosen can be chosen so that the frequencies of the first and

second clock are not integer multiples of each other. The same also applies to claim 24, wherein the limitation of using the circuit in a battery operated electronic device is seen to be intended use and is therefore not given any patentable weight.

Allowable Subject Matter

11. Claims 14-15 and 21-25 would be would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
CC
March 16, 2005

Terry D. Cunningham
Primary Examiner